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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
LTO.0504US

In Re Application Of: **Daniel Xu et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/976,641	**October 12, 2001**	**Bradley W. Baumeister**	**2815**

Invention: **Reducing Leakage Currents in Memories With Phase-Change Material**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **March 18, 2004.**

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Signature

Dated: **April 30, 2004**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Daniel Xu et al.	Art Unit:	2815
Serial No.:	09/976,641	Examiner:	Bradley W. Baumeister
Filed:	October 12, 2001		
For:	Reducing Leakage Currents in Memories With Phase-Change Material	Atty Docket:	ITO.0504US P12497

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APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed December 18, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Ovonyx, Inc.

II. RELATED APPEALS AND INTERFERENCES

None.

Date of Deposit: April 30, 2004
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III. STATUS OF THE CLAIMS

Claims 11-14 and 16-30 are rejected. Each rejection is appealed.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF THE INVENTION

Referring to Figure 1, a phase-change memory cell 10 may include a phase-change material 32 formed in a pore 24. The pore 24 may include an etched aperture formed through a dielectric material 30. In some embodiments, the walls of the dielectric material 30 and the pore 24 may be defined by a cylindrically shaped sidewall spacer 36. Thus, in some embodiments, the phase-change material 32 may coat the walls of the pore 24 defined by the sidewall spacer 36 and may come in contact with the lower electrode 18. An upper electrode 34 may be defined over the phase-change material 32.

Signals may be applied through the lower electrode 18 to the phase-change material 32 and on to the upper electrode 34. These signals may include set and reset signals to change the programmed state of the phase-change material 32 as well as read signals to read the programmed state. See specification at page 3, line 24 through page 4, line 15.

The signals are supplied to the lower electrode 18 through a buried wordline 22 in one embodiment. In accordance with one embodiment of the present invention, the buried wordline 22 includes a more lightly doped or an N- region 22a over a more heavily doped or N+ region 22b over a more lightly doped or N- region 22c. The substrate 12 may be more lightly doped or P- material and layer 20 may be more heavily doped or P+ material.

In accordance with some embodiments of the present invention, the configuration of the buried wordline 22 reduces leakage current under reverse bias conditions, thereby lowering the standby current needed for the memory cells 10. The lower buried wordline resistance may result in less voltage drop along the row lines, enhancing the programming operation efficiency and lowering the programming current in some embodiments. In addition, the resulting diode, made up of the layers 20 and 22, may have an increased Zener breakdown voltage.

Turning next to Figure 2, the formation of the memory cell 10 may begin by forming a pair of spaced trenches 16 in the substrate 12. The trenches 16 may isolate one wordline from adjacent wordlines that make up a memory array. The trenches 16 may be filled with an oxide 14 in some embodiments. The region between the trenches 16 may then be subjected to a series of ion-implantation steps, indicated at I.

As a result of a sequence ion-implantation steps, a diode formed of a P+ region 20 over an N type buried wordline 22 may be defined in a P- substrate 12. In particular, the energy, dose and doping profiles of a series of implants may be adjusted to achieve the sequence of layers 22a, 22b and 22c indicated in Figure 3. That is, the concentration profile resulting from a plurality of implants may be selected so as to create the specied series of doped layers 22 by adjusting the depth of each implant's concentration profile. See specification at page 4, line 16 through page 5, line 25.

While the exact nature of the ion-plantation steps may be subject to considerable variation, an initial implantation may be utilized to form a P type well. This may be followed by a P type and N type implant to form the buried wordline 22 and overlaying P+ region 20. These implants in turn may be followed by one or more additional implants, in some embodiments, to

create the profiles indicated in Figure 3. In some embodiments, the P type region may be formed by a boron implant and the N type region may be formed by a phosphorus implant.

Through the provision of the N- regions 22a and 22c, the reverse bias leakage current of the resulting cell 10 may be significantly improved in some embodiments. The implanted layers may be subjected to sufficient heat processing to achieve the desired performance.

A lower electrode layer 18 may be formed over the layers 20 and 22 as shown in Figure 4. In some embodiments, the lower electrode 18 may be formed of cobalt silicide. Thereafter, the cell 10 may be completed by defining the pore 24 and developing the structure shown in Figure 1. See specification at page 6, line 1 through page 7, line 8.

Referring to Figure 5, the memory 48, formed according to the principles described herein, may act as a system memory. The memory 48 may be coupled to a interface 44, for instance, which in turn is coupled between a processor 42, a display 46 and a bus 50. The bus 50 in such an embodiment is coupled to an interface 52 that in turn is coupled to another bus 54. See specification at page 7, lines 9 through 24.

VI. ISSUES

A. Is Claim 11 Obvious Over Ovshinsky, Chang, and Slotboom?

VII. GROUPING OF THE CLAIMS

All of the claims may be grouped with claim 11.

VIII. ARGUMENT

A. Is Claim 11 Obvious Over Ovshinsky, Chang, and Slotboom?

Claim 11 calls for a buried line formed in the substrate. That buried line includes a more lightly doped region over more heavily doped region and more lightly doped region.

The Examiner suggests that Ovshinsky teaches the more lightly doped region over a more heavily doped region. While this is true, the argument fails to teach the claim limitations. The claim limitation requires that the buried line be formed in the substrate. The buried line includes the lightly doped region over and under a more heavily doped region.

In Ovshinsky, the more lightly doped region is not formed in the substrate but, instead, is formed by an epitaxial layer formed over the substrate. As explained in column 15, line 60 *et seq.* of Ovshinsky "on top of this N+ grid structure is formed an N-doped crystalline epitaxial layer 14, again by techniques well known in the art." Thus, Ovshinsky fails to teach the more lightly doped region on top of a more heavily doped region formed in the substrate.

The same element is also missing from the Chang reference. It is plain that neither Chang nor Ovshinsky had any idea how to make a more lightly doped region over a more heavily doped region, as well as a more lightly doped region under the more heavily doped region or they failed to appreciate the reason to do so. To suggest that two references that fail to teach a more lightly doped region formed in the substrate over more heavily doped region also formed in the substrate can somehow teach the opposite begs the obviousness question.

In the Advisory Action, the Examiner argues the logically incorrect position that because someone taught putting a lightly doped region over a more heavily doped region and someone else taught putting a more heavily doped region over a more lightly doped region, having a sandwich of lightly doped, heavily doped, lightly doped, as claimed, is somehow obvious. Of course, that argument begs the obviousness question since there is no suggestion whatsoever to

make the claimed combination. Moreover, as pointed out above, the combination is not the simple addition of lightly over heavily and heavily over lightly. There has to be some way to make all three layers, which is not so simple. None of the references teach any way to form, in the bulk substrate, the three different layers over one another.

The assertion in the Advisory Action that the Applicant admitted that Ovshinsky teaches lightly over heavily doped regions may strictly be arguable, but it is clear that the Applicant never admitted that Ovshinsky teaches lightly over heavily doped regions in the bulk substrate.

Thus, the rejection must fail because nothing teaches any rationale to make the three layers claimed in the way claimed and nothing teaches how one would go about achieving the result only set forth in the claimed invention. More to the point, the combination of three references which teach, according to the Examiner, combinations of one lightly doped and one heavily doped layer indicate, if anything, that it was unobvious how to and why to make a combination of lightly over heavily over lightly doped, all in the bulk substrate. More likely, this was too difficult a proposition for any of the cited references.

The problem that must be overcome includes at least the following difficulty. One could implant into a p-type substrate an n-type material to make two layers of different doping concentrations. But to create three layers of different doping concentrations in the same substrate is not suggested by any of the references. A single implantation is simply not enough to achieve it.

Therefore, the rejection of claim 11 should be reversed.

IX. CONCLUSION

Applicants respectfully request that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: April 30, 2004

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APPENDIX OF CLAIMS

The claims on appeal are:

11. A memory cell comprising:

a substrate;

a phase-change material over said substrate;

a buried line of a first conductivity type formed in said substrate, said buried line including a more lightly doped region over a more heavily doped region and a more lightly doped region under said more heavily doped region;

a region of a second conductivity type opposite said first conductivity type over said line and under said phase-change material; and

a pair of trenches on either side of said buried line extending past said buried line and said region of a second conductivity type into said substrate under said buried line.

12. The memory cell of claim 11 including a dielectric material defining a pore over the substrate, said phase-change material being formed in said pore.

13. The memory cell of claim 12 including a contact layer under said dielectric layer aligned with said pore.

14. The memory cell of claim 13 wherein said lightly doped regions reduce the reverse bias leakage of said line.

16. The memory cell of claim 11 wherein said line is a wordline that couples to other memory cells.

17. The memory cell of claim 11 wherein said lightly doped regions are N-type material.

18. The memory cell of claim 17 wherein said lightly doped regions are N- regions.

19. The memory cell of claim 18 wherein said substrate is a P-type substrate.

20. The memory cell of claim 12 wherein said pore is lined with a sidewall spacer.

21. An electronic device comprising:

a system memory circuit including:

a substrate;

a phase-change material over said substrate;

a conductive line of a first conductivity type in said substrate, said line including a more heavily doped region sandwiched between more lightly doped regions, said conductive line providing signals to said phase-change material;

a region of a second conductivity type between said phase-change material and said conductive line;

a pair of trenches on either side of said buried line, said trenches extending through said substrate along said conductive line and said region of a second conductivity type into the substrate below said conductive line; and

a processor coupled to said system memory circuit.

22. The device of claim 21 wherein said phase-change material forms a memory cell of a storage.

23. The device of claim 22 wherein said storage is part of a computer.

24. The device of claim 22 including a processor, an interface and a bus coupled to said storage.

25. The device of claim 22 wherein said conductive line is a buried wordline.

26. The device of claim 25 including a conductive material between said phase-change material and said conductive line.

27. The device of claim 26 wherein said conductive line is formed of a material having a first conductivity type, a material of a second conductivity type being defined in said surface over said conductive line.

28. The device of claim 27 wherein said more heavily doped region is an N+ region and said more lightly doped regions are N- regions.

29. The device of claim 21 wherein said surface includes a semiconductor substrate.

30. The device of claim 29 including an insulator material positioned over said surface and a pore being formed in said insulator material, said phase-change material being formed in said pore.